INTERSIL

ICL8052/ICL71C03 Pair
and
ICL8068/ICL71C03 Pair

Precision 4½ Digit A/D Converter

FEATURES

- **Typically less than 2μV p-p noise (200.00mv full scale, ICL8068)**
- **Accuracy guaranteed to ±1 count over entire ±20,000 counts (2.0000 volts full scale)**
- **Guaranteed zero reading for 0 volts input**
- **True polarity at zero count for precise null detection**
- **Single reference voltage required**
- **Over-range and under-range signals available for auto-ranging capability**
- **All outputs TTL compatible**
- **Medium quality reference (40ppm typical) on board**
- **Blinking display gives visual indication of over-range**
- **Six auxiliary inputs/outputs are available for interfacing to UARTs, Microprocessors or other complex circuitry**
- **5pA input current typical (8052A)**
- **Pin compatible with the ICL7103**

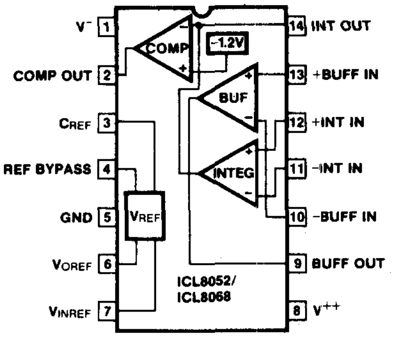
GENERAL DESCRIPTION

The ICL8052 or ICL8068/ICL71C03 chip pairs with their multiplexed BCD output and digit drivers are ideally suited for the visual display DVM/DPM market. The outstanding 4-1/2 digit accuracy, 200.00mV to 2.0000V full scale capability, auto-zero and auto-polarity combine with true ratiometric operation, almost ideal differential linearity and time-proven dual slope conversion. Use of these chip pairs eliminates clock feedthrough problems, and avoids the critical board layout usually required to minimize charge injection.

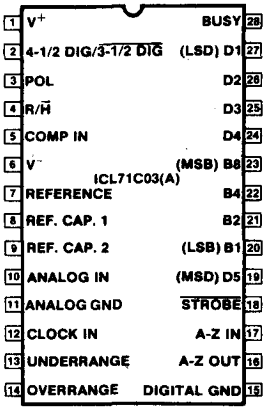
When only 2000 counts of resolution are required the 71C03 can be wired for 3-1/2 digits and give up to 30 readings/second making it ideally suited for a wide variety of applications.

The ICL71C03 is an improved CMOS plug-in replacement for the ICL7103 and should be used in all new designs.

PIN CONFIGURATION



(Outline dwg PD, DD)



(Outline dwg DI,JI,PI)

ORDERING INFORMATION

Part	Temp. Range	Package	Order Number
8052	0°C to 70°C	14 pin plastic DIP	ICL8052CPD
8052	0°C to 70°C	14 pin ceramic DIP	ICL8052CDD
8052A	0°C to 70°C	14 pin plastic DIP	ICL8052ACPD
8052A	0°C to 70°C	14 pin ceramic DIP	ICL8052ACDD
8068	0°C to 70°C	14 pin ceramic DIP	ICL8068CDD
8068A	0°C to 70°C	14 pin ceramic DIP	ICL8068ACDD

Part	Temp. Range	Package	Order Number
71C03	0°C to 70°C	28-Pin Plastic DIP	ICL71C03CPI
71C03	0°C to 70°C	28-Pin Ceramic DIP	ICL71C03CDI
71C03	0°C to 70°C	28-Pin CERDIP	ICL71C03CJI
71C03A	0°C to 70°C	28-Pin CERDIP	ICL71C03ACJI
71C03A	0°C to 70°C	28-Pin Plastic DIP	ICL71C03ACPI
71C03A	0°C to 70°C	28-Pin Ceramic DIP	ICL71A03ACDI

8068 ELECTRICAL CHARACTERISTICS ($V^{++} = +15V$, $V^{-} = -15V$, $T_A = 25°C$ unless otherwise specified)

CHARACTERISTICS	CONDITIONS	8068			8068A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
EACH OPERATIONAL AMPLIFIER								
Input Offset Voltage	$V_{CM} = 0V$		20	65		20	65	mV
Input Current (either input) (Note 1)	$V_{CM} = 0V$		175	250		80	150	pA
Common-Mode Rejection Ratio	$V_{CM} = \pm 10V$	70	90		70	90		dB
Non-Linear Component of Common-Mode Rejection Ratio (Note 2)	$V_{CM} = \pm 2V$		110			110		
Large Signal Voltage Gain	$R_L = 50k\Omega$	20,000			20,000			V/V
Slew Rate			6			6		V/μs
Unity Gain Bandwidth			2			2		MHz
Output Short-Circuit Current			5	10		5	10	mA
COMPARATOR AMPLIFIER								
Small-signal Voltage Gain	$R_L = 30k\Omega$		4000					V/V
Positive Output Voltage Swing		+12	+13		+12	+13		V
Negative Output Voltage Swing		−2.0	−2.6		−2.0	−2.6		V
VOLTAGE REFERENCE								
Output Voltage		1.5	1.75	2.0	1.60	1.75	1.90	V
Output Resistance			5			5		Ω
Temperature Coefficient			50			40		ppm/°C
Supply Voltage Range		±10		±18	±10		±18	V
Supply Current Total				14		8	14	mA

8052 ELECTRICAL CHARACTERISTICS ($V^{++} = +15V$, $V^{-} = -15V$, $T_A = 25°C$ unless otherwise specified)

CHARACTERISTICS	CONDITIONS	8052			8052A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
EACH OPERATIONAL AMPLIFIER								
Input Offset Voltage	$V_{CM} = 0V$		20	50		20	50	mV
Input Current (either input) (Note 1)	$V_{CM} = 0V$		5	50		2	10	pA
Common-Mode Rejection Ratio	$V_{CM} = \pm 10V$	70	90		70	90		dB
Non-Linear Component of Common-Mode Rejection Ratio (Note 2)	$V_{CM} = \pm 2V$		110			110		
Large Signal Voltage Gain	$R_L = 10k\Omega$	20,000			20,000			V/V
Slew Rate			6			6		V/μs
Unity Gain Bandwidth			1			1		MHz
Output Short-Circuit Current			20	100		20	100	mA
COMPARATOR AMPLIFIER								
Small-signal Voltage Gain	$R_L = 30k\Omega$		4000					V/V
Positive Output Voltage Swing		+12	+13		+12	+13		V
Negative Output Voltage Swing		−2.0	−2.6		−2.0	−2.6		V
VOLTAGE REFERENCE								
Output Voltage		1.5	1.75	2.0	1.60	1.75	1.90	V
Output Resistance			5			5		Ω
Temperature Coefficient			50			40		ppm/°C
Supply Voltage Range		±10		±18	±10		±18	V
Supply Current Total			6	12		6	12	mA

Note 1: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents are measured with junctions at ambient temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_J = T_A + \Theta_{jA}$ Pd where Θ_{jA} is the thermal resistance from junction to ambient. A heat sink can be used to reduce temperature rise.

Note 2: This is the only component that causes error in dual-slope converter.

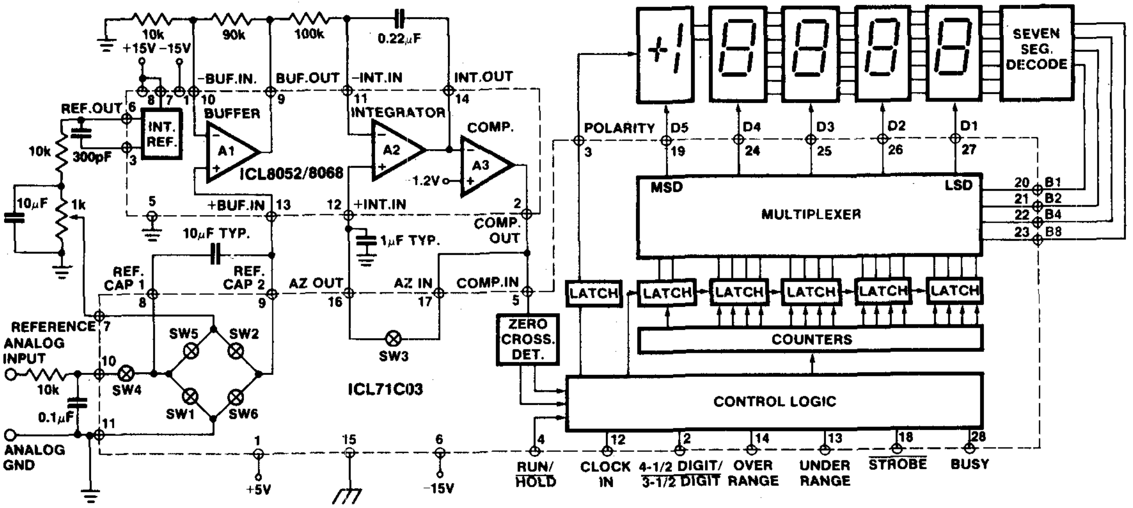


Figure 1. Functional Block Diagram

DETAILED DESCRIPTION

Analog Section

Figure 2 shows the equivalent Circuit of the Analog Section o both the ICL71C03/8052 and the ICL71C03/8068 in the 3 different phases of operation. If the RUN/HOLD pin is left open or tied to V+, the system will perform conversions at a rate determined by the clock frequency: 40,002 at 4-1/2 digit and 4002 at 3-1/2 digit clock periods per cycle (see Figure 3 for details of conversion timing).

1. **Auto-Zero Phase I** Fig. 2A.
During Auto-Zero, the input of the circuit is shorted to ANALOG GROUND through switch 1, and switch 3 closes a loop around the integrator and comparator, the purpose of which is to charge the auto-zero capacitor until the integrator output does not change with time. Also, switches 1 and 2 recharge the reference capacitor to V_{REF}.

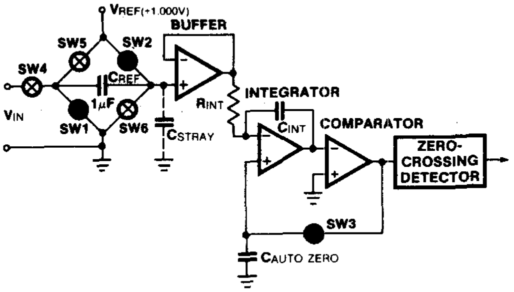


Figure 2A: Phase I Auto-Zero

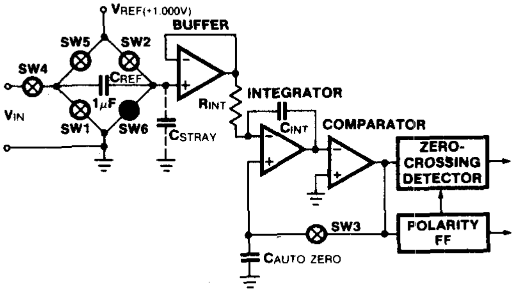


Figure 2C: Phase III + Deintegrate

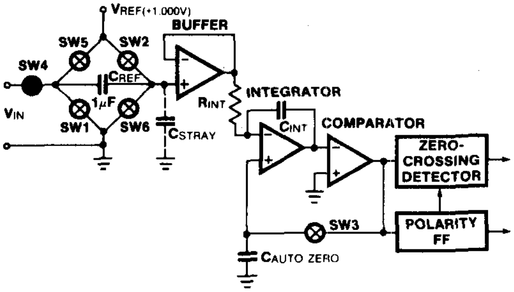


Figure 2B: Phase II Integrate Input

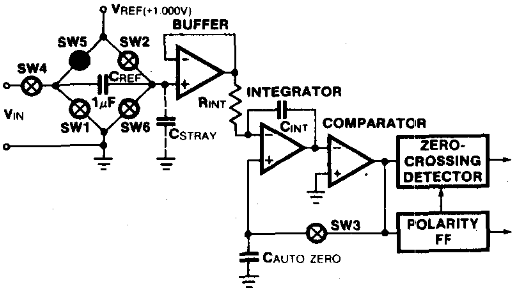


Figure 2D: Phase III - Deintegrate

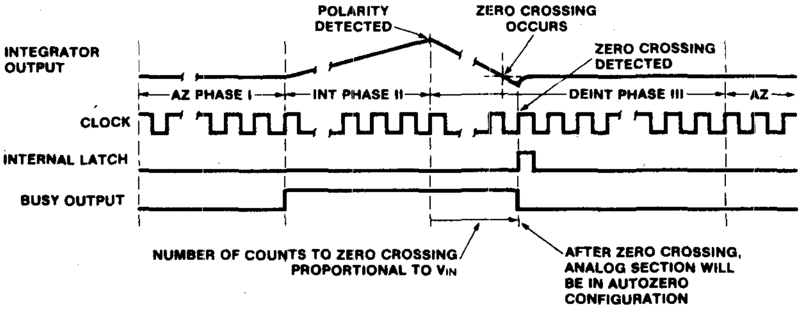
Figure 2: Analog Section of Either ICL8052 or ICL8068 with ICL71C03

2. Input Integrate Phase II Fig. 2B.

During Input Integrate the auto-zero loop is opened and the ANALOG INPUT is connected to the BUFFER INPUT through switch 4. If the input signal is zero, the buffer, integrator and comparator will see the same voltage that existed in the previous state (Auto-Zero). Thus, the integrator output will not change but will remain stationary during the entire Input Integrate cycle. If V_{IN} is not equal to zero, an unbalanced condition exists compared to the Auto-Zero phase, and the integrator will generate a ramp whose slope is proportional to V_{IN}. At the end of this phase, the sign of the ramp is latched into the polarity F/F.

3. Deintegrate Phase III Fig. 2C&D.

During the Deintegrate phase, the switch drive logic uses the output of the polarity F/F in determining whether to close switch 6 or 5. If the input signal is positive, switch 6 is closed and a voltage which is V_{REF} more negative than during Auto-Zero is impressed on the BUFFER INPUT. Negative inputs will cause $\pm V_{REF}$ to be applied to the BUFFER INPUT via switch 5. Thus, the reference capacitor generates the equivalent of a (+) or (−) reference from the single reference voltage with negligible error. The reference voltage returns the output of the integrator to the zero-crossing point established in Phase I. The time, or number of counts, required to do this is proportional to the input voltage. Since the Deintegrate phase can be twice as long as the Input Integrate phase, the input voltage required to give a full scale reading $= 2V_{REF}$.



COUNTS			
	Phase I	Phase II	Phase III
4-1/2 digit	10,001	10,000	20,001
3-1/2 digit	1,001	1,000	2,001

Figure 3: Conversion Timing

Zero-Crossing Flip Flop

Fig. 4 shows the problem that the zero-crossing F/F is designed to solve.

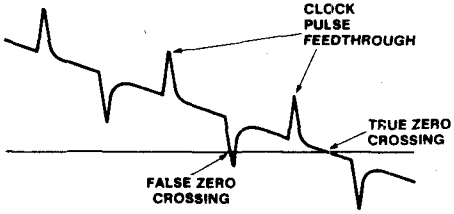


Figure 4: Integrator Output Near Zero-Crossing

The integrator output is approaching the zero-crossing point where the count will be latched and the reading displayed. For a 20,000 count instrument, the ramp is changing approximately 0.50mV per clock pulse (10 volt max integrator output divided by 20,000 counts). The clock pulse feedthrough superimposed upon this ramp would have to be less than 100μV peak to avoid causing significant errors.

The flip-flop interrogates the data once every clock pulse after the transients of the previous clock pulse and half-clock pulse have died down. False zero-crossings caused by clock pulses are not recognized. Of course, the flip-flop delays the true zero-crossing by one count in every instance, and if a correction were not made, the display would always be one count too high. Therefore the counter is disabled for one clock pulse at the beginning of phase 3. This one count delay compensates for the delay of the zero-crossing flip-flop, and allows the correct number to be latched into the display. Similarly, a one count delay at the beginning of phase 1 gives an overload display of 0000 instead of 0001. No delay occurs during phase 2, so that true ratiometric readings result

DETAILED DESCRIPTION

Digital Section

The 71C03 includes several pins which allow it to operate conveniently in more sophisticated systems. These include:

1. **4-1/2/$\overline{\text{3-1/2}}$ (Pin 2).** When high (or open) the internal counter operates as a full 4-1/2 decade counter, with a complete measurement cycle requiring 40,002 counts. When held low, the least significant decade is cleared and the clock is fed directly into the next decade. A measurement cycle now requires only 4,002 clock pulses. All 5 digit drivers are active in either case, with each digit lasting 200 counts with Pin 2 high (4-1/2 digit) and 20 counts for Pin 2 low (3-1/2 digit).

2. **RUN/$\overline{\text{HOLD}}$ (Pin 4).** When high (or open) the A/D will free-run with equally spaced measurement cycles every 40,002/4,002 clock pulses. If taken low, the converter will continue the full measurement cycle that it is doing and then hold this reading as long as Pin 4 is held low. A short positive pulse (greater than 300ns) will now initiate a new measurement cycle beginning with up to 10,001/1,001 counts of auto zero. Of course if the pulse occurs before the full measurement cycle (40,002/4,002 counts) is completed, it will not be recognized and the converter will simply complete the measurement it is doing. *An external indication that a full measurement cycle has been completed is that the first* $\overline{\text{STROBE}}$ pulse (see below) will occur 101/11 counts after the end of this cycle. Thus, if RUN/$\overline{\text{HOLD}}$ is low and has been low for at least 101/11 counts, the converter is holding and ready to start a new measurement when pulsed high.

3. **$\overline{\text{STROBE}}$ (Pin 18).** This is a negative-going output pulse that aids in transferring the BCD data to external latches, UARTs or microprocessors. There are 5 negative-going $\overline{\text{STROBE}}$ pulses that occur in the center of each of the digit drive pulses and occur once and only once for each measurement cycle starting 101/11 pulses after the end of the full measurement cycle. Digit 5 (MSD) goes high at the end of the measurement cycle and stays on for 201/21 counts. In the center of this digit pulse (to avoid race conditions between changing BCD and digit drives) the first $\overline{\text{STROBE}}$ pulse goes negative for 1/2 clock pulse width. Similarly, after Digit 5, Digit 4 goes high (for 200/20 clock pulses) and 100/10 pulses later the $\overline{\text{STROBE}}$ goes *negative for the second time.* This continues through Digit 1 (LSD) when the fifth and last $\overline{\text{STROBE}}$ pulse is sent. The digit drive will continue to scan (unless the previous signal was over-range) but no additional $\overline{\text{STROBE}}$ pulses will be sent until a new measurement is *available.*

4. **BUSY (Pin 28).** BUSY goes high at the beginning of signal integrate and stays high until the first clock pulse after zero-crossing (or after end of measurement in the case of an OVER-RANGE). The internal latches are enabled (i.e., loaded) during the first clock pulse after BUSY and are latched at the end of this clock pulse. The circuit automatically reverts to auto-zero when not BUSY so it may also be considered an $\overline{\text{A-Z}}$ signal. A very simple means for transmitting the data down a single wire pair from a remote location would be to AND BUSY with clock and subtract 10,001/1,001 counts from the number of pulses received — as mentioned previously there is one "NO-count" pulse in each Reference Integrate cycle.

5. **OVER-RANGE (Pin 4).** *This pin goes positive when the* input signal exceeds the range (20,000/2,000) of the converter. The output F-F is set at the end of BUSY and is *reset to zero at the beginning of* Reference Integrate in the next measurement cycle.

6. **UNDER-RANGE (Pin 13).** This pin goes positive when the reading is 9% of range or less. The output F-F is set at the end of BUSY (if the new reading is 1800/180 or less) and is reset at the beginning of Signal Integrate of the next reading.

7. **POLARITY (Pin 3).** This pin is positive for a positive input signal. It is valid even for a zero reading. In other words, +0000 means the signal is positive but less than the least significant bit. The converter can be used as a null detector by forcing equal (+) and (−) readings. The null at this point should be less than 0.1 LSB. This output becomes valid at the beginning of Reference Integrate and remains correct until it is revalidated for the next measurement.

8. **Digit Drives (Pins 19, 24, 25, 26 and 27).** Each digit drive is a positive-going signal which lasts for 200/20 clock pulses. The scan sequence is D_5 (MSD), D_4, D_3, D_2 and D_1 (LSD). All five digits are scanned even when operating in the 3-½ digit mode, and this scan is continuous unless an OVER-RANGE occurs. Then all Digit drives are blanked from the end of the $\overline{\text{STROBE}}$ sequence until the beginning of Reference Integrate, at which time D_5 will start the scan again. This gives a blinking display as a visual indication of OVER-RANGE.

9. **BCD (Pins 20, 21, 22 and 23).** The Binary coded decimal bits B_8, B_4, B_2 and B_1 are positive logic signals that go on simultaneously with the Digit driver.

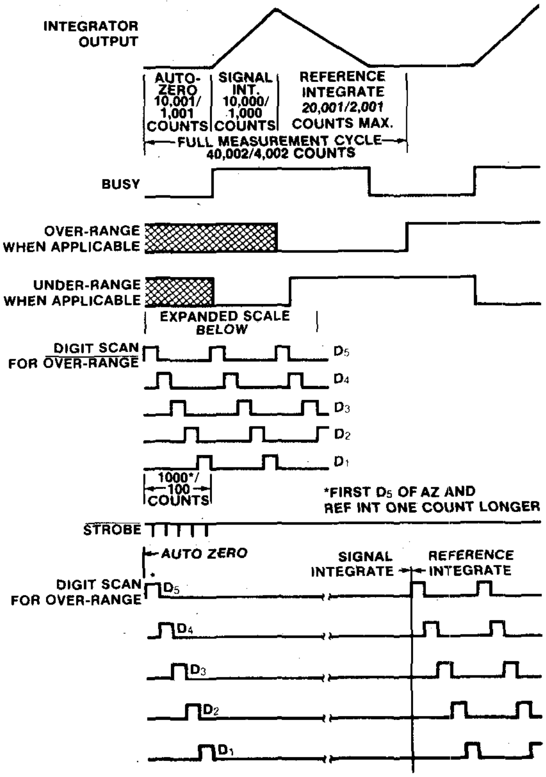


Figure 5: Timing Diagram for Outputs

COMPONENT VALUE SELECTION

For optimum performance of the analog section, care must be taken in the selection of values for the integrator capacitor and resistor, auto-zero capacitor, reference voltage, and conversion rate. These values must be chosen to suit the particular application.

Integrating Resistor

The integrating resistor is determined by the full scale input voltage and the output current of the buffer used to charge the integrator capacitor. This current should be small compared to the output short circuit current such that thermal effects are kept to a minimum and linearity is not affected. Values of 5 to 40μA give good results with a nominal of 20μA. The exact value may be chosen by

$$R_{INT} = \frac{\text{full scale voltage}^*}{20\mu A}$$

*Note: If gain is used in the buffer amplifier then -

$$R_{INT} = \frac{\text{(Buffer gain) (full scale voltage)}}{20\mu A}$$

Integrating Capacitor

The product of integrating resistor and capacitor is selected to give 9 volt swing for full scale inputs. This is a compromise between possibly saturating the integrator (at +14 volts) due to tolerance build-up between the resistor, capacitor and clock and the errors a lower voltage swing could induce due to offsets referred to the output of the comparator. In general, the value of C_{INT} is given by

$$C_{INT} = \frac{\left[\begin{matrix}10{,}000 \text{ (4-1/2 digit)}\\ 1000 \text{ (3-1/2 digit)}\end{matrix} \times \text{clock period}\right] \times (20\mu A)}{\text{Integrator output voltage swing}}$$

A very important characteristic of the integrating capacitor is that it has low dielectric absorption to prevent roll-over or ratiometric errors. A good test for dielectric absorption is to use the capacitor with the input tied to the reference.

This ratiometric condition should read half scale 1.0000, and any deviation is probably due to dielectric absorption. Polypropylene capacitors give undetectable errors at reasonable cost. Polystyrene and polycarbonate capacitors may also be used in less critical applications.

Auto-Zero and Reference Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system, a large capacitor giving less noise. The reference capacitor should be large enough such that stray capacitance to ground from its nodes is negligible.

Note: When gain is used in the buffer amplifier the reference capacitor should be substantially larger than the auto-zero capacitor. As a rule of thumb, the reference capacitor should be approximately the gain times the value of the auto-zero capacitor. The dielectric absorption of the reference cap and auto-zero cap are only important at power-on or when the circuit is recovering from an overload. Thus, smaller or cheaper caps can be used here if accurate readings are not required for the first few seconds of recovery.

Reference Voltage

The analog input required to generate a full scale output is $V_{IN} = 2\ V_{REF}$.

The stability of the reference voltage is a major factor in the overall absolute accuracy of the converter. For this reason, it is recommended that an external high quality reference be used where the ambient temperature is not controlled or where high-accuracy absolute measurements are being made.

Buffer Gain

At the end of the auto-zero interval, the instantaneous noise voltage on the auto-zero capacitor is stored, and subtracted from the input voltage while adding to the reference voltage during the next cycle. The result of this is that the noise voltage is effectively somewhat greater than the input noise voltage of the buffer itself during integration. By introducing some voltage gain into the buffer, the effect of the auto-zero noise (referred to the input) can be reduced to the level of the inherent buffer noise. This generally occurs with a buffer gain of between 3 and 10. Further increase in buffer gain merely increases the total offset to be handled by the auto-zero loop, and reduces the available buffer and integrator swings, without improving the noise performance of the system. The circuit recommended for doing this with the ICL8068/ICL71C03 is shown in Figure 6.

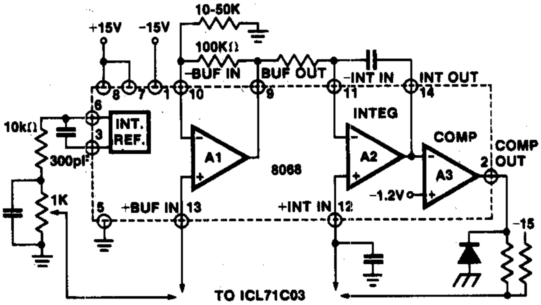


Figure 6: Adding Buffer Gain to ICL8068

ICL8052 vs ICL8068

The ICL8052 offers significantly lower input leakage currents than the ICL8068, and may be found preferable in systems with high input impedances. However, the ICL8068 has substantially lower noise voltage, and is the device of choice for systems where noise is a limiting factor, particularly in low signal level conditions.

Max Clock Frequency

The maximum conversion rate of most dual-slope A/D converters is limited by the frequency response of the comparator. The comparator in this circuit is no exception, even though it is entirely NPN, with an open-loop gain-bandwidth product of 300MHz. The comparator output follows the integrator ramp with a 3μs delay, and at a clock frequency of 160kHz (6μs period) half of the first reference integrate clock period is lost in delay. This means that the meter reading will change from 0 to 1 with a 50μV input, 1 to 2 with 150μV, 2 to 3 at 250μV, etc. This transition at mid-point is considered desirable by most users. However, if the clock frequency is increased appreciably above 160kHz, the instrument will flash "1" on noise peaks even when the input is shorted.

For many dedicated applications where the input signal is always of one polarity, the delay of the comparator need not be a limitation. Since the non-linearity and noise do not increase substantially with frequency, clock rates of up to ~1MHz may be used. For a fixed clock frequency, the extra count or counts caused by comparator delay will be a constant and can be subtracted out digitally.

The minimum clock frequency is established by leakage on the auto-zero and reference caps. With most devices, measurement cycles as long as 10 seconds give no measurable leakage error.

To achieve maximum rejection of 60Hz pickup, the signal integrate cycle should be a multiple of 60Hz. Oscillator frequencies of 300kHz, 200kHz, 150kHz, 120kHz, 100kHz, 40kHz, 33-1/3kHz, etc. should be selected. For 50Hz rejection, oscillator frequencies of 250kHz, 166-2/3kHz, 125kHz, 100kHz, etc. would be suitable. Note that 100kHz (2.5 readings/second) will reject both 50 and 60Hz.

The clock used should be free from significant phase or frequency jitter. A simple two-gate oscillator and one based on a CMOS 7555 timer are shown in the Applications section. The multiplexed output means that if the display takes significant current from the logic supply, the clock should have good PSRR.

APPLICATIONS

Specific Circuits Using the 8068/71C03 8052/71C03

Figure 7 shows the complete circuit for a ±4-1/2 digit (±200.0mV full scale) A/D with LED readout using the internal reference of the 8068/52. If an external reference is used, the reference supply (pin 7) should be connected to ground and the 300pF reference cap deleted. The circuit also shows a typical R-C input filter. Depending on the application, the time-constant of this filter can be made faster, slower, or the filter deleted completely. The 1/2 digit LED is driven from the 7 segment decoder, with a zero reading blanked by connecting a D5 signal to RBI input of the decoder.

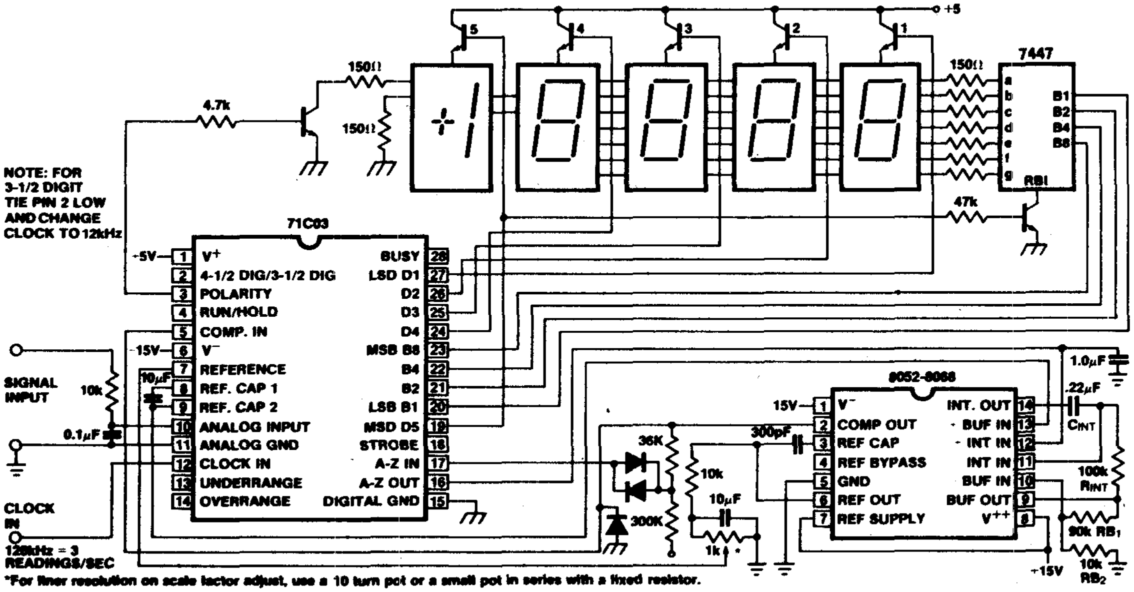
A voltage translation network is connected between the comparator output of the 8068/52 and the auto-zero input of the 71C03. The purpose of this network is to assure that, during auto-zero, the output of the comparator is at or near the threshold of the 71C03 logic (+2.5V) while the auto-zero capacitor is being charged to V_{REF} (+100.0mV for a 200.0mV instrument). Otherwise, even with zero volts in, some reference integrate period would be required to drive the comparator output to the threshold level. This would show up as an equivalent offset error. Once the divider network has been selected, the unit-to-unit variation should contribute less than a tenth of a count error. A second feature is the back-to-back diodes, used to lower the noise. In the normal operating mode they offer a high impedance and long integrating time constant to any noise pulses charging the auto-zero cap. At startup or recovery from an overload, their impedance is low to large signals so that the cap can be charged up in one auto-zero cycle. The buffer gain does not have to be set precisely at 10 since the gain is used in both the integrate and deintegrate phase. For scale factors other than 200.00mV the gain of the buffer should be changed to give a ±2V buffer output. For 2.0000V full scale this means unity gain and for 20,000mV (1μV resolution) a gain of 100 is necessary.* Not all 8068As can operate properly at a gain of 100 since their offset should be less than 10mV in order to accommodate the auto-zero circuitry. However, for devices selected with less than 10mV offset, the noise performance is reasonable with approximately 1.5μV near full scale. On all scales less than 200.00mV, the voltage translation network should be made adjustable as an offset trim.

The auto-zero cap should be 1μF for all scales and the reference capacitor should be 1μF times the gain of the buffer amplifier. At this value if the input leakages of the 8052/8068 are equal, the droop effects will cancel giving zero offset. This is especially important at high temperature. Some typical component values are shown in the table below. For 3-1/2 digit conversion use 12kHz clock.

$V^{++} = +15V$, $V^{+} = 5V$, $V^{-} = -15V$, Clock Freq = 120kHz (4-1/2 digit)

ICL8052/8068 with	ICL71C03A			UNITS
Full scale V_{IN}	20	200	2000	mV
Buffer Gain $\frac{(RB1 + RB2)}{RB2}$	100*	10	1	
R_{INT}	100	100	100	kΩ
C_{INT}	0.22	0.22	0.22	μF
C_{AZ}	1.0	1.0	1.0	μF
C_{REF}	10	10	1.0	μF
V_{REF}	10	100	1000	mV
Resolution (4-1/2 digit)	1	10	100	μV

*Note comment on offset limitations above. Buffer gain does not improve ICL8052 noise performance adequately.



*For finer resolution on scale factor adjust, use a 10 turn pot or a small pot in series with a fixed resistor.

Figure 7: 8052A (8068A)/71C03A 4-1/2 Digit A-D Converter

A suitable circuit for driving a plasma-type display is shown in Fig. 8. The high voltage anode driver buffer is made by Dionics. The 3 AND gates and caps driving 'BI' are needed for interdigit blanking of multiple-digit display elements, and can be omitted if not needed. The 2K & 3K resistors set the current levels in the display. A similar arrangement can be used with 'Nixie'® tubes.

® Nixie is a registered trademark of Burroughs Corporation.

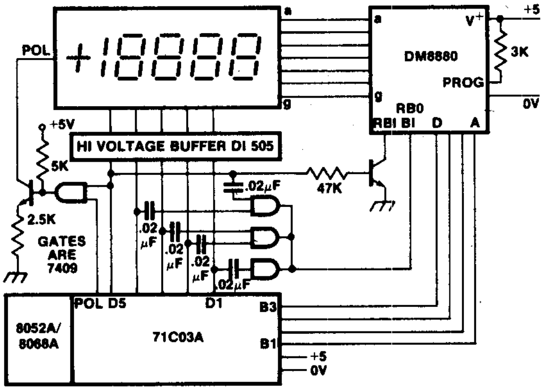


Figure 8: ICL8052-8068/71C03A Plasma Display Circuit

ANALOG AND DIGITAL GROUNDS

Extreme care must be taken to avoid ground loops in the layout of 8068 or 8052/71C03A circuits, especially in high sensitivity circuits. It is most important that return currents from digital loads are not fed into the analog ground line. Both of the above circuits have considerable current flowing in the digital ground returns from drivers, etc. A recommended connection sequence for the ground lines is shown in Figure 9.

Other Circuits for Display Applications

The popular LCD displays can be interfaced to the O/P of the ICL71C03 with suitable display drivers, such as the ICM7211A as shown in Figure 10. A standard CMOS 4000 series LCD driver circuit is used for displaying the 1/2 digit, the polarity, and an 'overange' flag. A similar circuit can be used with the ICM7212A LED driver and the ICM7235A vacuum fluorescent driver with appropriate arrangements made for the 'extra' outputs. Of course, another full driver circuit could be ganged to the one shown if required. This would be useful if additional annunciators were needed.

The Figure shows the complete circuit for a 4-1/2 digit (±2.000V) A/D again using the internal reference of the 8052A/8068A.

Figure 11 shows a more complicated circuit for driving LCD displays. Here the data is latched into the ICM7211 by the $\overline{\text{Strobe}}$ signal and 'Overange' is indicated by blanking the 4 digits. A clock oscillator circuit using the ICM7555 CMOS timer is shown. Some other suitable clock circuits are suggested in Figs. 12 & 13. The 2-gate circuit should use CMOS gates to maintain good power supply rejection.

A problem sometimes encountered with the 8052/68/71C03 A/D is that of gross over-voltage applied to the input. Voltage in excess of ±2.000 volts may cause the integrator output to saturate. When this occurs, the integrator can no longer source (or sink) the current required to hold the summing junction (Pin 11) at the voltage stored on the auto zero capacitor. As a result, the voltage across the integrator capacitor decreases sufficiently to give a false voltage reading. This problem can also show up as large-signal instability on overange conditions. A simple solution to this problem is to use junction FET transistors across the integrator capacitor to source (or sink) current into the summing junction and prevent the integrator amplifier from saturating, as shown in Figure 14.

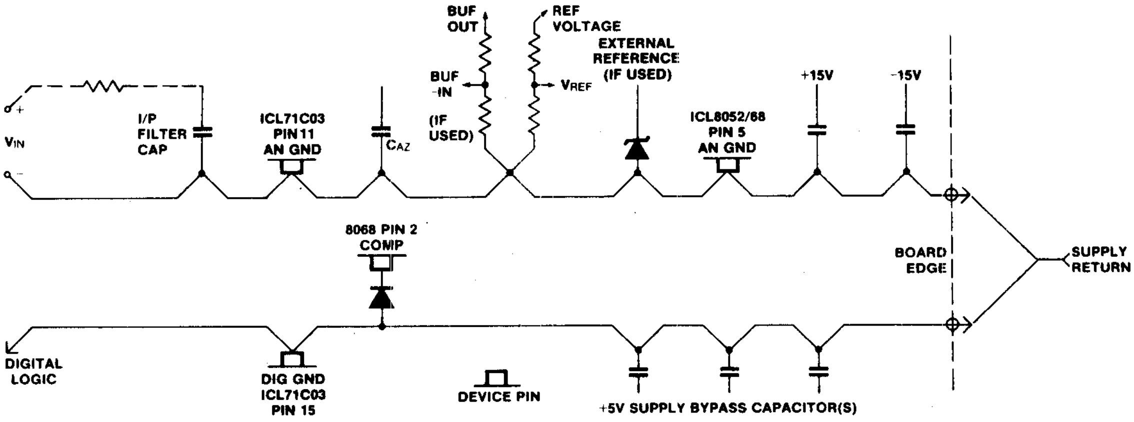


Figure 9: Grounding Sequence

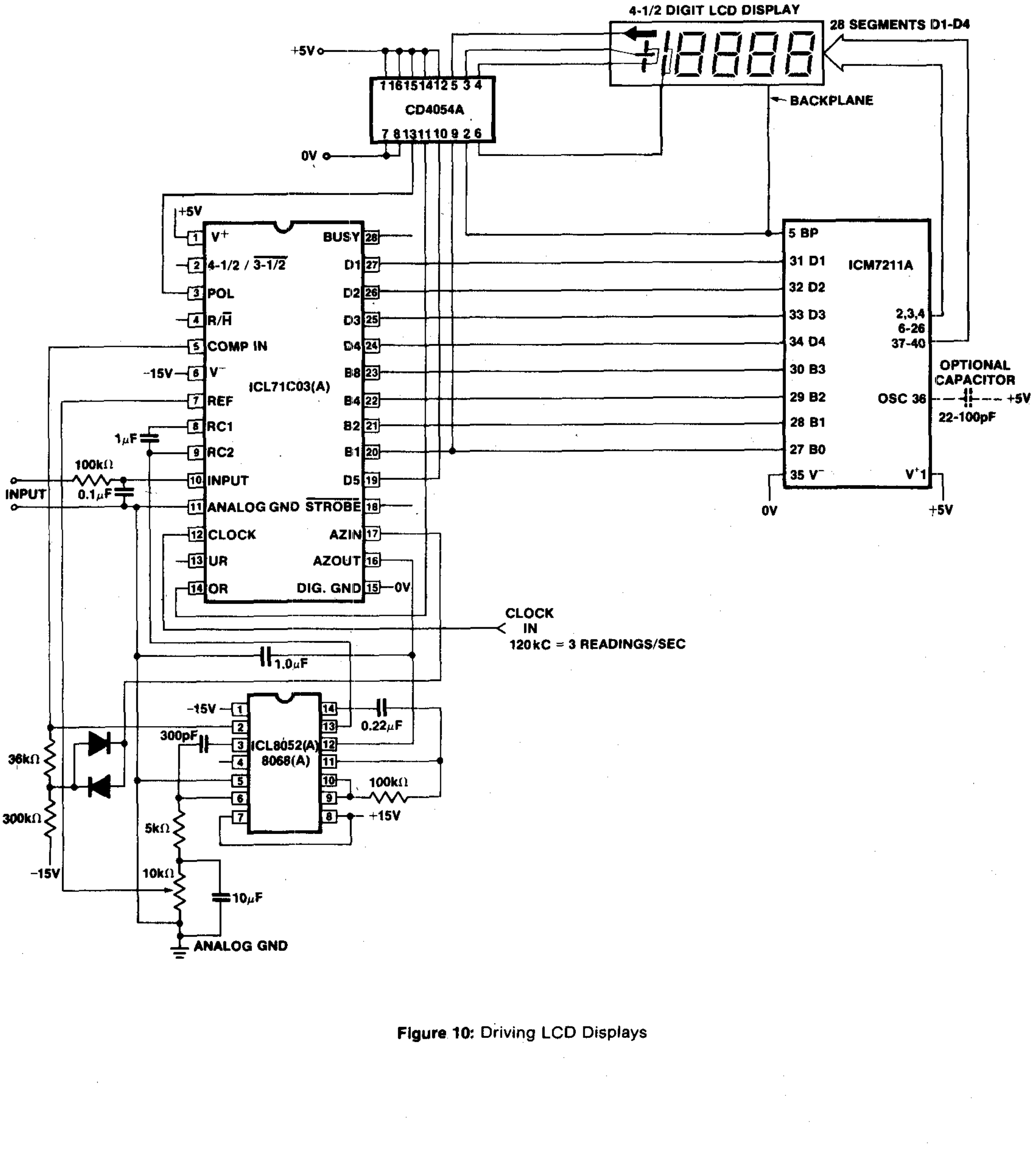


Figure 10: Driving LCD Displays

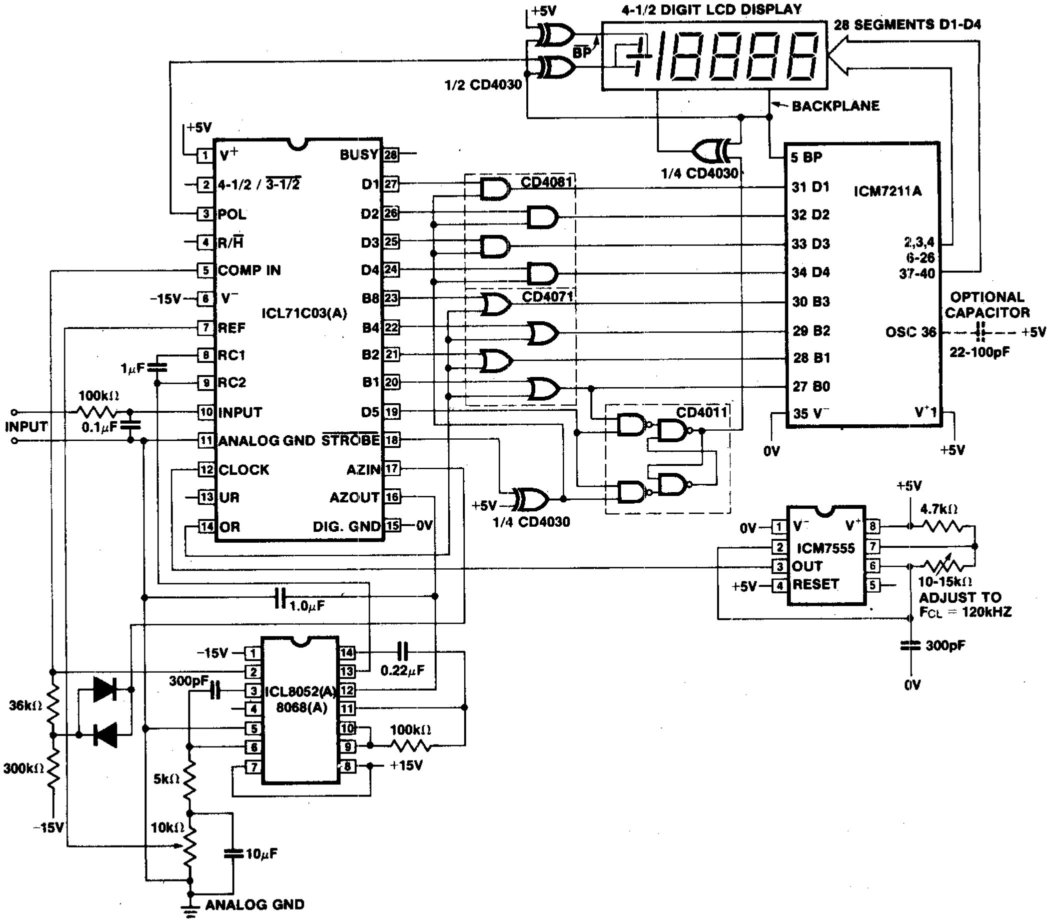


Figure 11: 4-1/2 Digit LCD DPM with Digit Blanking on Overrange.

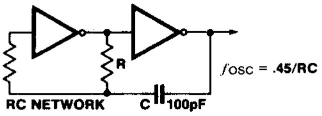


Figure 12

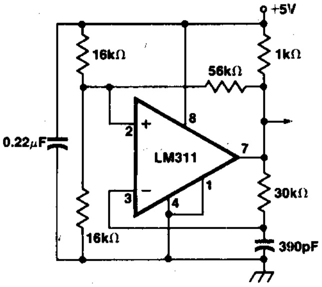


Figure 13: Clock Circuits

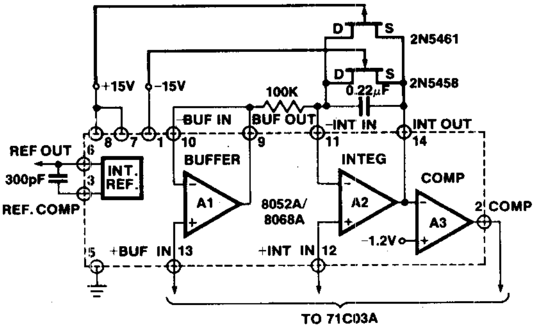


Figure 14: Gross Overvoltage Protection Circuit

INTERFACING WITH UARTS AND MICROPROCESSORS

Figure 15 shows a very simple interface between free-running 8068/8052/71C03A and a UART. The five Strobe pulses start the transmission of the five data words. The digit 5 word is 0000XXXX, digit 4 is 1000XXXX, digit 3 is 0100XXXX, etc. Also the polarity is transmitted indirectly by using it to drive the Even Parity Enable Pin (EPE). If EPE of the receiver is held low, a parity flag at the receiver can be decoded as a positive signal, no flag as negative. A complex arrangement is shown in Figure 16. Here the UART can instruct the A/D to begin a measurement sequence by a word on RRI. The Busy signal resets the Data Ready Reset (DRR). Again Strobe starts the transmit sequence. A quad 2 input multiplexer is used to superimpose polarity, over-range, and under-range onto the D_5 word since in this instance it is known that $B_2 = B_4 = B_8 = 0$.

For correct operation it is important that the UART clock be fast enough that each word is transmitted before the next $\overline{\text{STROBE}}$ pulse arrives. Parity is locked into the UART at load time but does not change in this connection during an output stream.

Circuits to interface the 71C03(A) directly with three popular microprocessors are shown in Figures 17, 18 and 19. The main differences in the circuits are that IM6100 with its 12 bit word capability can accept polarity, over-range, under-range, 4 bits of BCD and 5 digits simultaneously where the 8080/8048 and the MD6800 groups with 8 bit words need to have polarity, over-range and under-range multiplexed onto the Digit 5 word - as in the UART circuits. In each case the microprocessor can instruct the A/D when to begin a measurement and when to hold this measurement.

APPLICATION NOTES

A016	"Selecting A/D Converters," by David Fullagar
A017	"The Integrating A/D Converters," by Lee Evans
A018	"Do's and Don'ts of Applying A/D Converters," by Peter Bradshaw and Skip Osgood
A019	"4-1/2 Digit Panel Meter Demonstrator/Instrumentation Boards," by Michael Dufort
A023	"Low Cost Digital Panel Meter Designs," by David Fullagar and Michael Dufort
A028	"Building an Auto-Ranging DMM Using the 8052A/7103A A/D Converter Pair," by Larry Goff
R005	"Interfacing Data Converters & Microprocessors," by Peter Bradshaw et al, Electronics, Dec. 9, 1976

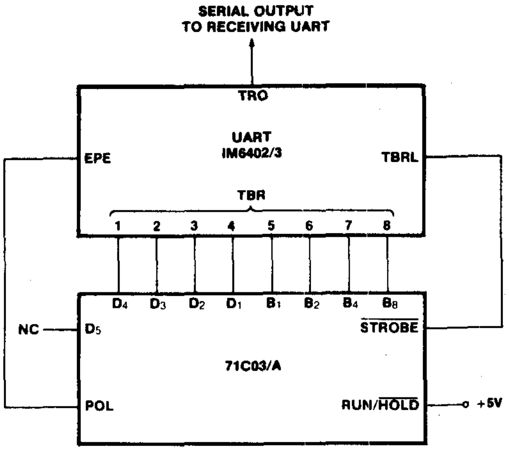


Figure 15: Simple 71C03/71C03A to UART Interface

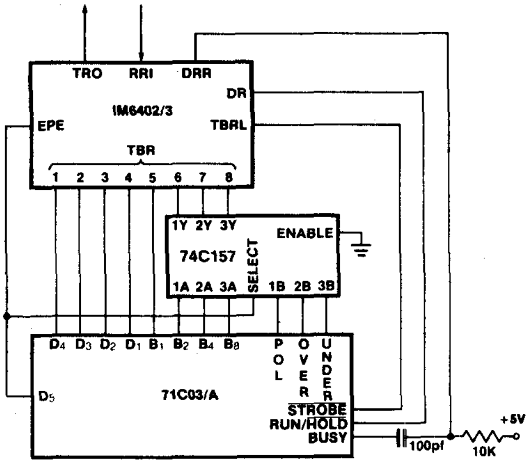


Figure 16: Complex 71C03/7103A to UART Interface

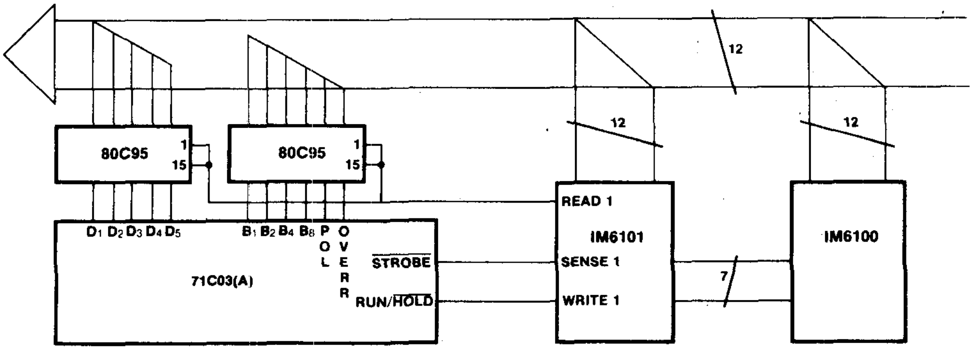


Figure 17: IM6100 to 71C03/71C03A Interface

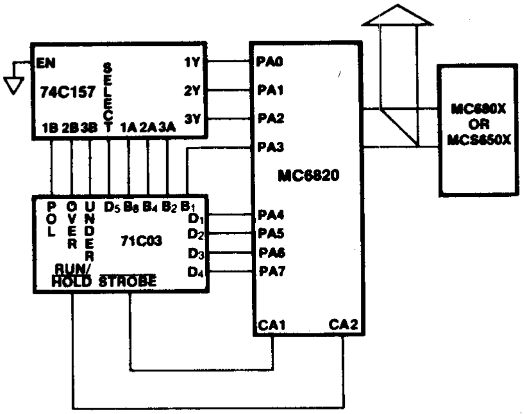


Figure 18: ICL71C03 to MC6800, MCS650X Interface

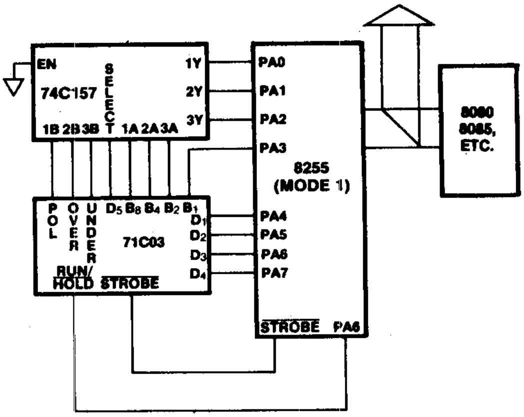


Figure 19: ICL71C03 to MCS-48, -80, 85 Interface